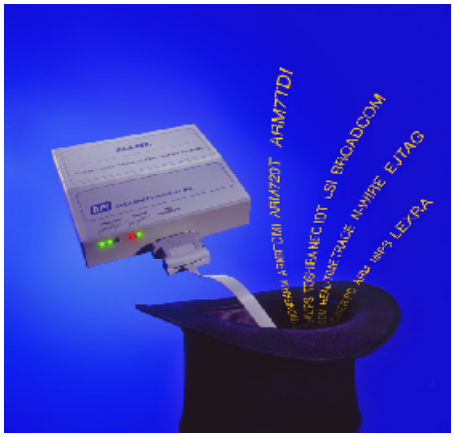
MAJIC™ MDS² Development System Features:

- **Ideal for multiple core SoC applications**
- **Provides EPI MDS² technology**
- **Supports execution tracing with on-chip trace buffers**
- **FLASH memory programming support**
- **Supports a wide choice of on-chip debug interfaces**
- **Supports a wide variety of CPU cores**
- **Supports on-chip hardware breakpoints**
- **Unlimited software breakpoints**
- **Programmable JTAG clock (TCK = 0 to 40 MHz)**
- **Programmable trigger-in and trigger-out connections**
- **Ethernet and serial I/O ports for fast, flexible host interface**
- **High speed download of application code**
- **Network compatibility allows shared and remote operation**
- **Internal RISC processor provides on-probe intelligence**
- **Wide choice of Configuration Kits extends usage to multiple architectures**



MAJIC™

- **Sleep-mode support**
- **LEDs display operation status**
- **Operates with most third party debuggers via industry standard APIs**
- **Optional EDB integrated debugger**
- **Interfaces for popular OS environments**

PRODUCT INFORMATION

Finally a non-intrusive debug solution for your multiple core SoC and high CPU pipeline speed designs. Now, you can have the same level of control and visibility of the embedded CPU as you would with in-circuit emulators in traditional discrete CPU designs. The result is faster software integration, better testing, and improved time to market.

The MAJIC^{MX} is the latest model in the MAJIC Series of intelligent debug probes. The series now supports scaling of SoC devices to unlimited clock rates and to unlimited number of on-chip cores. MAJIC^{MX} embodies the new EPI MDS^2 debug concept. This concept allows fast integration and debugging of software for complex SoC devices. It recognizes that SoC designs are rapidly scaling up in both pipeline speeds and complexity. Thus, MDS^2 supports:

Multi-tap devices,
Multi-core devices,
Multi-architecture environments,
Multi-session debug,
Multi-context CPUs, and
On-chip trace buffers.

The MAJIC^{MX} emulator provides a high-speed hardware interface between processors with an on-chip debug interface and industry standard debuggers. It is available with a choice of EPI debuggers and may be used with task-aware debuggers from leading OS vendors. The unit is self-contained in a small case approximately 2 x 6.5 x 7.5 inches in size.

The non-intrusive MAJIC^{MX} communicates with the CPU core by JTAG interface using the existing boundary scan pins. For most on-chip debug facilities, it uses no target memory and requires no porting to the target system.

Complete processor control means you can start, stop and single-step execution; read and write to registers, memory, and system I/O; and download code to target RAM – all within most industry standard debugger interfaces.

Built-in memory tests assist in hardware testing. And the EPI open-source flash programming algorithm allows programming of flash memory located either internal or external to the SoC device.

The MAJIC^{MX} expands to support additional cores, debug interfaces, or SoC devices. This eliminates the need to buy new emulators for each new project, thus reducing project costs.

You may adapt the MAJIC^{MX} for operation with your specific processor or CPU cores by selecting from a wide range of configuration kits. The kits contain the firmware and user license to match your CPU's on-chip debug facilities. Install multiple configuration kits, and the MAJIC^{MX} will support a variety of CPU types.

The MAJIC^{MX} is ready to run with the EPI software tools and any development board that supports a connection to the on-chip debug interface. This combination of tools will work together to provide you with a proven working environment.

The MAJIC^{MX} is available as a stand-alone unit or as a complete emulation kit. The kit contains serial and Ethernet cables, source-level debugger, and one year of free maintenance, support, and updates. Part number: MAJIC^{MX}-KIT.

Complete development kits are also available that include a compilation toolkit. See the EPI Price and Configuration Guide for full details of these development kits.

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Features of the MAJIC^{MX} include:

Multi-Dimensional Scaling Support for SoC Devices

MAJIC^{MX} embodies the new MDS^2 debug concept. This concept allows fast integration and debugging of software for complex SoC devices. To support SoC designs that are rapidly scaling up in both pipeline speeds and complexity, MAJIC^{MX} supports:

Multi-tap devices,
Multi-core devices,
Multi-architecture environments,
Multi-session debug,
Multi-context CPUs, and
On-chip trace buffers.

Request the EPI MDS^2 application note for more details.

Execution Tracing

MAJIC^{MX} supports full execution tracing from CPU cores that offer on-chip trace buffers. Trace control allows tracing from start of execution or tracing up to a breakpoint.

Ethernet Interface

The 10Base-T/100Base-T Ethernet interface provides many advantages over serial or parallel interfaces to the host. Download of your application code is over ten times faster than with serial interface. This will significantly reduce the amount of time spent waiting for code changes to download to your target board.

Network connection allows remote operation of the MAJIC^{MX}. Now you can access the lab setup directly from your desktop. This allows multiple engineers to share a common test bench.

Flash Memory

The MAJIC^{MX} firmware is easily upgraded without the need to replace ROMs.

Quickly install new configuration kits to add support for multiple CPU types and easily program IP address into the unit for point to point Ethernet operation.

Internal RISC Processor

A high performance internal RISC processor provides fast response to debugger operations such as single-stepping and downloading code to the target.

MAJIC^{PLUS} Version Includes Trace Buffer

For cores that require an off-chip trace memory, see the MAJIC^{PLUS} data sheet.

Choice of Configuration Kits

You may configure the MAJIC^{MX} to support one or more of the supported combinations of CPU core and on-chip debug interface. Each configuration kit includes the firmware, user license and interconnections necessary to support the CPU that you have chosen. Please refer to the Configuration Kit data sheet for detailed specifications on the CPUs and on-chip interfaces currently supported.

Programmable JTAG Clock

The MAJIC^{MX} features a programmable TCK with a 0 to 40 MHz range. This allows you to tailor the JTAG operation to match the performance of your target. It also means that you can use the MAJIC^{MX} with low speed ASIC emulators, with FPGA implementation of your SoC design, or with devices that feature sleep mode operation.

Convenient Reset Switch

A convenient reset button on the MAJIC^{MX} is protected against accidental activation, yet is easily accessible by the user when a complete system reset is desired.

Programmable Trigger Control

The MAJIC^{MX} gives you control over both the trigger-in and trigger-out signals. The trigger-in signal may be used to create a breakpoint or synchronize execution. A trigger output may set to indicate execution status, indicate memory accesses, or indicate a memory test failure.

Status LEDs

The MAJIC^{MX} provides five LEDs, which show the operational status of the emulator. These LEDs also indicate the results of the built-in self-test that is automatically performed upon startup.

International Power Supply

The MAJIC^{MX} operates from a standard 5V power source. It comes with an external UL/CE approved AC adapter whose AC input range is compatible with all international AC voltage and frequency ranges. A standard three-wire power connector is compatible with readily available power cords through the world.

Specifications:

MAJIC^{MX}

JTAG clock(TCK):	0 to 40 MHz, programmable
Download speed:	>100k bytes/sec (typical)
Target voltage:	1.8 to 5.0V
Serial interface:	RS232C 1900-115.2k baud
Ethernet interface:	10/100base-T, TCP/IP
Triggers:	Trigger input, Trigger output
Trigger control	
Trigger in:	Off, run sync, break
Trigger out:	Off, run sync, memory access, memory test error
Trigger levels:	TTL
Indicator LEDs:	Power, status, run, connect, Ethernet
Size:	2.0 H x 7.4 W x 6.5 L (inches)
Weight:	2.25 lbs
Input power:	5 VDC +/- 5%, 4.0 A
Power connector:	2.1 mm coaxial, center positive, male
Temperature:	Operating 0 - 40 degrees C
Humidity:	Operating 15% - 95% RH
Safety/EMC:	CE

External AC Adapter

Output:	5 VDC, 4.0 A
Input voltage:	90 - 264 VAC
Input frequency:	47 - 63 Hz
Input power:	0.8 A
Size:	1.6 H x 2.8 W x 4.8 L (inches)
Weight:	10.3 oz
Compliance:	UL, CUL, CE, TUV
AC connector:	EN 60320/13
DC connector:	2.1 mm coaxial, center positive, female